PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)
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Peer SCHMITT	) Group Art Unit: 2827
	)
Serial No.: 10/791,834	) Examiner: Thong Quoc Le
	)
Filed: March 4, 2004	) Attorney Docket No. 003921.00148
	)
For: TERNARY BIT LINE SIGNALING	)

REQUEST FOR RECONSIDERATION

U.S. Patent and Trademark Office
Customer Service Window – Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

This paper is responsive to the non-final Office Action mailed February 4, 2005. Reconsideration and allowance are respectfully requested in view of the following remarks. Please charge any fees due to our Deposit Account No. 19-0733.

Claims 1-9 remain pending. Claims 1-3 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,104,663 to Kablanian ("Kablanian"). Claims 1-9 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,804,143 to Hobson ("Hobson"). Applicant respectfully traverses all rejections.

Independent Claim 1

Claim 1 recites a memory device, comprising a plurality of addressable memory cells, each memory cell configured to store a first bit and a second bit. Each claimed memory cell includes, among other features, a first storage circuit configured to store the first bit, and a second storage circuit configured to store the second bit. To assist the Examiner in understanding the claim, reference is made, for example, to the illustrative embodiment of Fig. 2 in Applicant's specification. In that embodiment, storage circuit 214 may be compared with the claimed first storage circuit and storage circuit 213 may be compared with the claimed second

storage circuit.

Claim 1 additionally recites that the second storage circuit is coupled to the first storage circuit and configured to deactivate the first storage circuit based on the second bit. For example, referring to Fig. 2 again, storage circuit 214 is deactivated based on the bit stored at node 231 of storage circuit 213 (via transistor 212).

Kablanian discloses a pair of cells 502, 504 (Fig. 5) that each stores a single bit. However, as confirmed by a simple inspection of the schematic of Fig. 5, neither of these cells is deactivated based on the bit stored at the other one of these bit cells. In fact, the bit stored in one of the bit cells 502, 504 has absolutely no effect on whether the other one of the bit cells is deactivated. Thus, Kablanian fails to teach or suggest, a second storage circuit configured to deactivate the first storage circuit based on the second bit, as recited in claim 1.

The Office Action refers to specific portions of Kablanian, none of which teach or suggest this claim recitation. The Office Action refers to col. 4, lines 7-26, which states that port A or port B can either be idle or writing. However, there is no teaching or suggestion that the states of ports A and B are based on the bit stored in a cell. More precisely, this portion of Kablanian does not teach or suggest deactivating one of the cells 502, 504 based on the bit stored in the other cell. The Office Action also refers to col. 7, lines 43-67, and col. 8, lines 1-7, which describe the input/output circuit of Fig. 6, but which has nothing to do with the cells 502, 504 of Fig. 5 that are asserted by the Office Action. Thus, it is not surprising that this portion of Kablanian also fails to teach or suggest deactivating one of the cells 502, 504 based on the bit stored in the other cell.

As to Hobson, a pair of bit cells 50, 48 is shown in Fig. 10 that each stores a single bit. However, as again confirmed by a simple inspection of the schematic of Fig. 10, neither of these bit cells in Hobson is deactivated based on the bit stored at the other one of these bit cells. Like Kablanian, the bit stored in one of the bit cells 50, 48 has absolutely no effect on whether the other one of the bit cells is deactivated. Thus, Hobson also fails to teach or suggest, a second storage circuit configured to deactivate the first storage circuit based on the second bit, as recited

in claim 1.

The Office Action refers to col. 6, lines 25-67 of Hobson. This portion states that "only one cell can be written to at any particular time, as determined by the logic values applied to the mutually exclusive read/write enable lines. Similarly, only one cell can be read from at any particular time." Again, this portion fails to teach or suggest that deactivation would be based on one of the bits stored in one of the bit cells. Instead, this portion describes how one may choose which cell to read from or write to depending upon the values of the read/write enable lines. The read/write enable lines are enable lines, not bits stored in the bit cells.

For at least these reasons, nether Kablanian nor Hobson anticipates claim 1. Applicant therefore respectfully requests allowance of claim 1.

Independent Claim 6

Independent claim 6 recites an apparatus, comprising a plurality of dual-bit memory cells. Each claimed memory cell includes (1) a first storage circuit configured to store a first bit, (2) a second storage circuit configured to store a second bit, (3) a first plurality of word lines each controlling one of the first storage circuits, and (4) a second plurality of word lines each controlling one of the second storage circuits. In addition, the first storage circuit includes a transistor having a gate, and the gate is coupled to the second storage circuit so as to receive a value of the second bit.

To assist the Examiner's understanding of this claim, reference is made, for example, to the illustrative embodiment of Fig. 2 in Applicant's specification. In that embodiment, storage circuit 214 has a transistor 212, which has a gate coupled to storage circuit 213 so as to receive a value of the bit stored at node 231.

Hobson fails to teach or suggest the claimed transistor. The Office Action refers to Fig. 10 of Hobson, which shows two bit cells 50, 48 each having two transistors. None of these transistors has a gate configured as claimed. In particular, a simple inspection of Fig. 10 reveals that none of these gates are coupled to the other bit cell so as to receive a value of the bit stored

in that other bit cell, as required by claim 6. As for the transistors on the left side of Fig. 10, each of their gates is coupled to a read/write enable line. As for the transistors on the right side of Fig. 10, each of their gates is coupled to a write assist line.

For at least these reasons, Hobson fails to anticipate claim 6. Applicant therefore respectfully requests allowance of claim 6.

Dependent Claims

The remaining dependent claims are also allowable by virtue of their dependence from allowable independent claims, and further in view of the additional features recited therein.

For example, claim 4 further recites a first inverter having an input, an output, and an output enable; a second inverter having an input, an output, and an output enable, the first and second inverters forming a first latch; and a first transistor having a source and drain coupled between the output enables of the first and second inverters and a fixed potential, and a gate coupled to the second storage circuit. However, none of the four transistors in Fig. 10 of Hobson has a source and a drain coupled between output enables of inverters and a fixed potential. Nor do any of the four transistors have a gate coupled to the other bit cell.

As another example, claim 5 further recites that the gate of the first transistor of claim 4 is coupled to a node of a second latch of the second storage circuit. Again, none of the four transistors in Fig. 10 of Hobson has a gate coupled to a node of any storage circuit at all. Instead, the gates are clearly coupled to either a read/write enable line or to a write assist line.

As another example, claim 9 recites that the apparatus of claim 6 further includes a bit line pair each coupled to one of the memory cells, each bit line pair coupled to logic that combines the respective bit line pair into a single logical value. The asserted embodiment in Fig. 10 of Hobson is completely at odds with this recitation. As plainly shown in Fig. 10, there is no bit line pair coupled to each bit cell. Instead, each bit cell has a read/write bus and a write assist line. Since there is no bit line pair in this embodiment of Hobson, there would also be no need for logic to combine a bit line pair into a single logical value.